Design of Telescopic Cascode Amplifier with DC Gain 58 dB

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ABSTRACT

This paper presents a single stage telescopic cascode operational amplifier design in cadence 55nm CMOS technology. The circuits provide single ended output because of mirror pole implemented. It implements current mirror at the cascode stage. The mirror poles also limit it performance. The current mirror features also provide single output. The input of the operational amplifier is fully differential, while output is single ended. The cadence simulation in spectre show that the amplifier can attain a open loop DC gain of 58dB, while the phase margin of 62.11 degree. The amplifier power consumption is 43 nW at supply voltage of 1-V and gain-bandwidth product (GBW) of 3.8 MHz. Due to the low power consumption of the amplifier, it is implemented inside the VCO based delta-sigma modulator analog-to-digital converter. Due to the telescopic topology, the signal swing at the output of the amplifier is quite small and its power consumption is lowered.

Keywords: Telescopic cascode, mirror, DC gain, GBW, Operational amplifier.

1. INTRODUCTION:

An amplifier is an important building block for the analog signal as the output of the transducer quite small. To enhance the signal swing, to be used for the analog-to-digital converter. The amplifier allows to implement cascode configuration. The performance of the Delta sigma ADC depends upon the specifications of the operational amplifier. The Gain bandwidth, the open loop Gain of operational amplifier, phase margin and slew rate are the performance parameters of the operational amplifier. The amplifier allows to implement cascode configuration. The complete amplifier simulated at the transistor level in the cadence can achieve open loop DC gain of 58 dB and GBW of 3.8 MHz. In this paper [1] a gain boosted fully differential telescopic cascode operational amplifier is designed. The main operational amplifier has a switch capacitor common mode feedback circuit and it's a fully differential OP Amp. The boosting Op Amp is also fully differential, but it has a continuous time CMFB circuit. The supply voltage of operational amplifier is 3.3V while this process is done in SMIC 0.35u mixed signal CMOS technology. The operational Amplifier attain a 129dB of open loop dc gain and a

unity gain frequency of 161MHz. The phase margin of this op amp is 70.4 degree. In this paper [2] there are three different fully differential and complementary self-biased CMOS operational amplifiers is presented and analyzed. These three Op Amp are based on telescopic cascode, folded cascode and single stage inverter based are discussed. These topologies are self-biased through negative feedback in bias loop and thus the need of voltage reference is eliminated. This adaptive biasing attenuates the supply voltage, process and variations in temperature. The folded cascode operational amplifier also increase the immunity towards common mode components within input signal. All these three types of operational amplifiers are analyzed by means of low frequency calculations and circuit implementations. A novel class-AB design for single stage amplifier is presented in this paper [3]. For the creation of class-AB behavior a switch capacitor level shifter structure is employs to apply to both sink and source output transistors. We can eliminate a current mirror circuit of traditional class-AB structure by using the structure that is discussed in previous line. Finally, we can save some power and operation frequency can also be increased. The results of simulations show that fast settling telescopic cascode operational amplifier with this pseudo class AB method confirm that this approach reduce the power consumption. To increase slew rate this technique can be applied to first of the two stages of operational amplifier. A high-performance high swing CMOS operational amplifier is designed in this paper [4]. To achieve high swing of operational amplifier the tail and current source transistors in deep linear region. This will result the degradation in the differential gain, common mode rejection ratio and other characteristics of amplifier are compensated by applying replica tail feedback method and regulated-cascode differential gain enhancement. The simulation is performed in 0.8um CMOS technology. The supply voltage of this op amp is 3.3V. It attains an open loop differential gain of 90dB while the unity gain frequency of 90MHz and CMRR more then 50dB. Through analytical and simulation results, is shows that op amp attains its higher CMRR at high frequencies also. For front end readout ASIC, a nested-current mirror recycling folded cascode OTA is designed in this paper [5]. For the improvement of output impedance and small signal transconductance a nested current mirror technology is applied to recycling folded cascode amplifier. It also improves the gain bandwidth DC gain and slew rate. The presented amplifier designed using 0.11um CMOS technology. After simulations this amplifier attain DC gain of 76.44, gain bandwidth of 90.02 and slew rate of 93.64. So finally, it improves 26MHz of GBW 69V/us in slew rate and 22dB of DC gain as compared to conventional RFC amplifier. Due to better output swing and relaxed headroom a folded cascade operational amplifier is preferred 1st stage choice in two stage op amp. Because of folding transistors, the gain and noise of this op amp is compromised. In this paper [6] FVF assisted differential pair has been presented which extract signal and inject it on the gate of folding devices and hence gain and noise will reduce. This simulation is performed in 28nm CMOS technology, and the post layout simulation was also performed. The presented operational amplifier attains a DC gain of 68dB also provide improvement 20% in input referred noise while the power consumption is same as

conventional op amp. The power consumption of this circuit is 33uW with power supply of 1V.A novel architecture of folded cascode OTA is designed in this paper [7] for 10-bit pipeline analog to digital converter. Folded cascode operational transconductance amplifier is main block of pipelined ADCs. It has a stable transient output of 1.6 volt. This operational amplifier provides the open loop gain of 42.78dB while the CMRR is 43.11dB slew rate of 105.657V/us and phase margin of 133^0. The amplifier is deigned in 0.18um CMOS technology with the supply voltage of 1.8V and the power consumption is of 13.64uW. This power consumption is low as compared to the conventional folded cascode OTA. Bioelectrical signal acquisition system used to amplify, record, store and process data. The one of the most important stages is amplification. An Operational transconductance amplifier is designed in this paper [8] by using 0.18um CMOS technology. Interdigitated method was employed to improve the chip area and to reduce the parasitic capacitances. This amplifier polarized at 1.8Volt. The op Amp attain a open loop gain of 53.40dB with gain bandwidth of 10mHz to 2.21kHz. The common mode rejection ratio is of 82.17dB while the PSRR is of 105.65dB. The input referred noise is of 236 nV/Hz. According to these characteristics this OTA can be used for LFP, EEG or ECoG biopotential amplifiers.

2. MATERIALS AND METHODS

In order to attain a high gain, we can use the differential cascode techniques. This telescopic cascode is one of them. This circuit is a single ended output with differential input. We can attain much higher gain, but the output swing is low. We also must add some additional poles. The schematic diagram of this circuit is show in the figure 1.

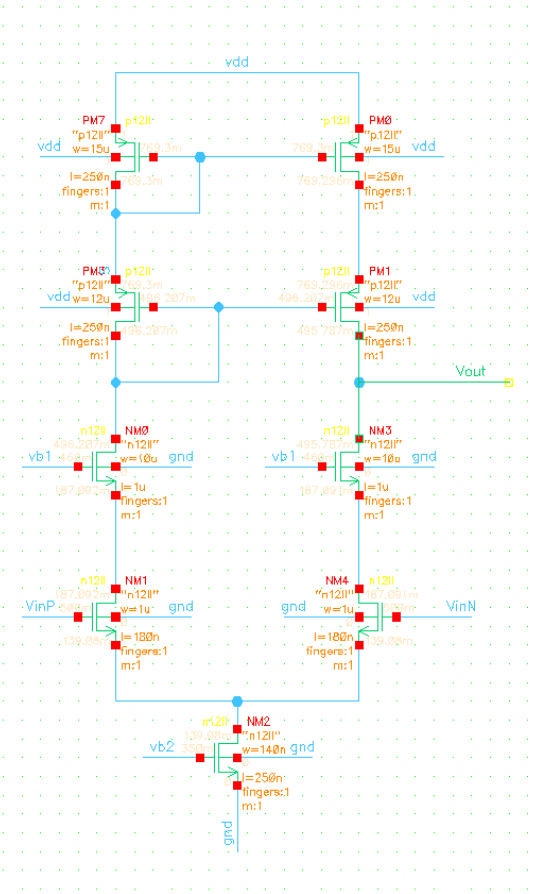

Figure 1

In this circuit a two-mirror pole is added and node X and Y. The supply voltage is applied to this operational amplifier is 1 Volt. The input of this Op Amp is differential while the output is single ended. After simulation this circuit attain a gain of 58dB while the phase margin of 62.11^0. The gain bandwidth of this amplifier is 3. 8MHz.The power consumption of this circuit is only 43.26nW.

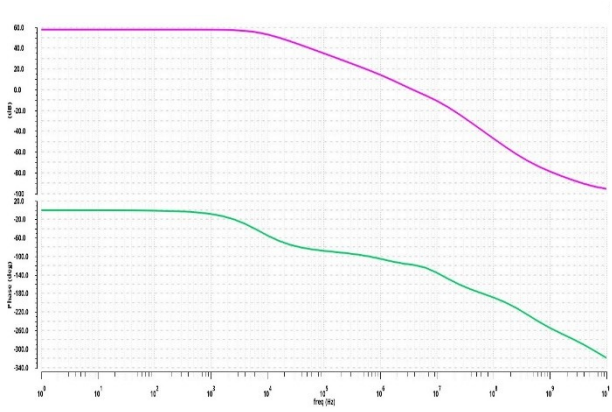

Figure 2

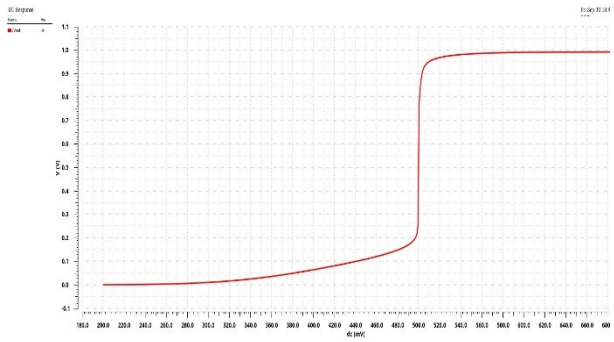

Figure 3

The figure 2 show the open loop gain and phase of this operational amplifier. While in the figure 3 the DC transfer curve is mentioned. From this DC transfer curve, we can find the offset voltage Whose value is 97mV. Then we perform simulations for DC gain. By using the calculator of cadence, we find the value of DC gain which is 520.57 V/V. The plot of the DC gain is shown in the figure 4.

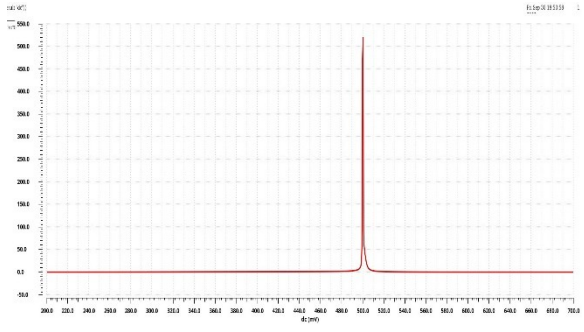

Figure 4

For the calculation of slew rate, we perform simulations by using transient analysis and finally we find slew rate of 1.578 V/µs. The transient response is shown in the figure 5. All the performance parameters are shown in the table below.

Parameters	Values
Open loop gain	58dB
Phase margin	62.11^0
Offset voltage	97mV
DC gain	520.57 V/V
Slew Rate	1.578 V/µs

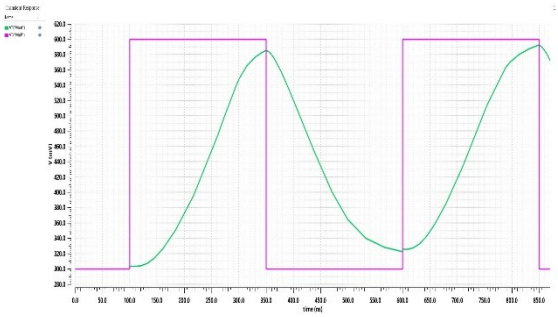

Figure 5

3. CONCLUSION

A telescopic cascode single stage amplifier designed in Cadence can achieve open loop gain of 58 dB and GBW of 3.8 MHz. The phase margin of the amplifier is 62.11^0. The DC simulations of the amplifier is also performed for the calculations of DC gain slew rate and offset voltage. It will provide the DC gain of 520.57V/V while the offset voltage is of 97mV, and the slew rate is 1.578 V/µs. The performance of the amplifier shows that it can consumes power of 43 nW at supply voltage of 1-V.

4. REFERENCES

[1] ***Wang*** **Jin and Qiu Yulin**, "Analysis and design of fully differential gain-

boosted telescopic cascode opamp," *Proceedings. 7th International Conference on Solid-State and Integrated Circuits Technology, 2004.*, 2004, pp. 1457-1460 vol.2

[2] **V. Milovanović and H. Zimmermann**, "On fully differential and complementary single-stage self-biased CMOS differential amplifiers," *Eurocon 2013*, 2013, pp. 1955-1963.

[3] **M. Taherzadeh-Sani, R. Lotfi and O. Shoaei,** "A pseudo-class-AB telescopic-cascode operational amplifier," *2004 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2004,

[4] **K. Gulati and Hae-Seung Lee**, "A high-swing CMOS telescopic operational amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2010-2019, Dec. 1998

[5] **D. Liu, T. Wei, S. Chen and N. Chen**, "An Improved Recycling Folded-Cascode Amplifier with Nested Current Mirror for Front-end Readout ASIC," *2022 IEEE 2nd International Conference on Electronic Technology, Communication and Information (ICETCI)*, 2022, pp. 281-284

[6] **R. Kumar, R. Nagulapalli and S. K. Vishvakarma**, "A Novel Gain Enhanced Folded Cascode OPAMP in 28nm CMOS Technology," *2022 International Conference on Electrical, Computer and Energy Technologies (ICECET)*, 2022, pp. 1-4.

[7] **D. S. Shylu Sam, P. S. Paul and D. Jayanthi**, "A Novel architecture of a Low Power Folded Cascode OTA in 180nm CMOS process," *2021 7th International Conference on Advanced Computing and Communication Systems (ICACCS)*, 2021, pp. 95-99

[8] **M. López-Solis *et al.*,** "High PSRR Folded Cascode OTA for Neural Signal Applications," *2021 IEEE 3rd International Conference on Circuits and Systems (ICCS)*, 2021, pp. 185-189